What is claimed is:

Sub B'

1. A controller for monitoring a temperature of an integrated circuit, comprising:

a first interface for receiving a first value representative of a temperature of said integrated circuit;

a second interface for receiving a second value representative of a threshold temperature; and

a comparator for comparing said first value to said second value for determining whether said first value exceeds said second value, thereby determining if said first value indicates an excessive temperature of said integrated circuit.

2. The controller of claim 1, further comprising a temperature measurement buffer for holding said first value received from said first interface.

3. The controller of claim 2, further comprising a serial temperature capture device for receiving a plurality of temperatures of said integrated circuit and sequentially providing said plurality of temperatures of said integrated circuit to said temperature measurement buffer.

4. The controller of claim 3, wherein said serial temperature capture device is adapted to receive a plurality of temperatures from a plurality of thermal sensors.

5. The controller of claim 3, further comprising a threshold buffer corresponding to said temperature measurement buffer and adapted to store a second value representative of a threshold temperature.

6. The controller of claim 5, wherein said threshold buffer is located external to said controller.

7. The controller of claim 2, wherein said temperature measurement buffer is adapted to receive said first value by way of a single wire.

8. The controller of claim 2, wherein said temperature measurement buffer is adapted to receive said first value by way of a plurality of wires.

9. The controller of claim 2, further comprising a microprocessor adapted to communicate with said temperature measurement buffer to read said first value and thermally profile said integrated circuit.

10. The controller of claim 2, wherein said temperature measurement buffer is located external to said controller.

11. The controller of claim 1, further comprising:

a plurality of temperature measurement buffers, wherein each temperature measurement buffer is adapted to receive a value representative of a temperature of an integrated circuit.

12. The controller of claim 11, wherein at least one of said plurality of temperature measurement buffers is located external to said controller.

13. The controller of claim 11, further comprising:

a serial temperature capture device for receiving a plurality of temperatures of said integrated circuit and providing said plurality of temperatures of said integrated circuit to said plurality of temperature measurement buffers.

14. The controller of claim 11, wherein at least one of said plurality of said temperature measurement buffers adapted to receive said first value by way of a single wire.

15. The controller of claim 11, wherein at least one of said plurality of said temperature measurement buffers is adapted to receive said first value by way of a plurality of wires.

16. The controller of claim 11, further comprising a microprocessor adapted to communicate with said plurality of temperature measurement buffers to read said values representative of temperatures of an integrated circuit and thermally profile said integrated circuit.

17. The controller of claim 11, further comprising a plurality of threshold buffers corresponding to said plurality of temperature measurement buffers and adapted to store a plurality of second values representative of threshold temperatures.

18. The controller of claim 1, further comprising a comparator response logic coupled to said comparator for determining whether an over-temperature condition in said integrated circuit exists.

19. The controller of claim 18, further comprising:

a window size buffer adapted to store a window size value and coupled to said comparator response logic;

wherein said comparator response logic operates as an up/down counter, counting said over-temperature conditions and determining whether an over-temperature condition in said integrated circuit exists when said up/down counter reaches said window size value.

20. The controller of claim 18, further comprising:

a window size buffer adapted to store a window size value and coupled to said comparator response logic;

wherein said comparator response logic operates as a counter, counting said over-temperature conditions occurring sequentially and determining whether an over-temperature condition in said integrated circuit exists when said counter reaches said window size value.

21. The controller of claim 18, wherein said comparator response logic uses digital filtering to filter said first value representative of a temperature of said integrated circuit.

22. The controller of claim 18, further comprising a response buffer coupled to said comparator response logic for storing a value representative of a response to said over-temperature condition.

23. The controller of claim 22, wherein said response comprises one of the group of assert an over-temperature pin, assert an over-temperature bit in an error buffer of said controller, assert an over-temperature bit in an error buffer of said microprocessor, issue an over-temperature interrupt to a service bus of said integrated circuit, cause a trap, slow an operating frequency of said integrated circuit, stop said integrated circuit, and do nothing.

24. The controller of claim 22, further comprising an interface from said response buffer to a microprocessor to enable said microprocessor to write to said response buffer.

25. The controller of claim 24, further comprising said microprocessor.

26. The controller of claim 18, further comprising an interface from said comparator response logic to a microprocessor to enable said microprocessor to communicate with said comparator response logic.

27. The controller of claim 26, further comprising said microprocessor.

28. The controller of claim 1, further comprising an interface from said first interface to a microprocessor to enable said microprocessor to read said first interface.

29. The controller of claim 1, further comprising an interface from said second interface to a microprocessor to enable said microprocessor to write to said second interface.

30. A controller for monitoring a temperature of an integrated circuit, comprising:

means for receiving a plurality of first values representative of a temperature of said integrated circuit;

means for comparing said plurality of first values to a plurality of corresponding second values representative of a plurality of threshold temperatures;

means for determining whether an over-temperature condition of said integrated circuit exists based on an output of said means for comparing.

31. The controller of claim 30, further comprising means for determining a response to said over-temperature condition.

32. The controller of claim 31, further comprising means for digitally filtering said output of said means for comparing before determining whether an over-temperature condition of said integrated circuit exists.

33. The controller of claim 30, further comprising a microprocessor capable of reading said means for receiving a plurality of first values and communicating with said means for determining whether an over-temperature condition of said integrated circuit exists.

34. The controller of claim 33, wherein said microprocessor is capable of writing to said means for receiving a plurality of first values and verifies correct functioning of the controller.

35. A method for monitoring a temperature of an integrated circuit, comprising the acts of:

receiving a plurality of first values representative of a temperature of said integrated circuit;

comparing said plurality of first values to a plurality of corresponding second values representative of a plurality of threshold temperatures;

determining whether an over-temperature condition of said integrated circuit exists based on a result of said act of comparing.

36. The method of claim 35, further comprising the act of determining a response to said over-temperature condition.

37. The method of claim 36, further comprising, before said act of determining whether an over-temperate condition of said integrated circuit exists, the act of digitally filtering said result of said act of comparing.

38. The method of claim 36, further comprising the act of executing said response to said over-temperature condition.